



PATENT APPLICATION 41/A
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2/11/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul W. Campbell
Serial No. 09/352,959
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Examiner: Pierre M. Vital
Art Group: 2186
Our File No. 00100.99.0094
Docket No. 0100.9900940

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Title: **METHOD AND APPARATUS FOR VIRTUAL ADDRESS TRANSLATION**

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Washington, D.C. 20231

I hereby certify that this paper is being sent via first class mail to: Box Fee Amendment, Commissioner for Patents, Washington, D.C. 20231 on this date.

Attn: Examiner Pierre M. Vital

1/29/03
Date:

Margaret Caruso
Margaret Caruso

AMENDMENT AND RESPONSE

Dear Sir:

In response to the Office Action mailed August 29, 2002 Applicant respectfully submit the following Amendment and Response.

In the Specification:

Please replace the paragraph on page 1, beginning at line 17, with the following rewritten paragraph:

Figure 1 illustrates a schematic block diagram of a portion of a computer system. As shown, a central processing unit is coupled to cache memory and to a north bridge. The north bridge is coupled to memory, an accelerated graphics port (AGP) bus, and a peripheral component interconnect (PCI) bus. The central processing unit addresses memory in system virtual address space, or linear address space. To communicate with the north bridge, the central processing unit converts addresses in virtual address space to addresses in physical address